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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

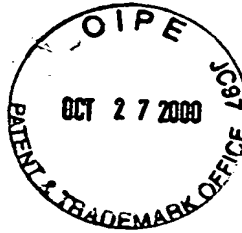
In re Application

Inventor(s): OM P. AGRAWAL et al.

SC/Serial No.: 09/235,615

Filed: January 21, 1999

Title: FPGA INTEGRATED CIRCUIT HAVING EMBEDDED  
SRAM MEMORY BLOCKS WITH REGISTERED  
ADDRESS AND DATA INPUT SECTIONS



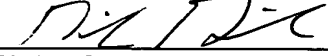
) PATENT APPLICATION

) Art Unit: 2819

) Examiner: D. Chang

**CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8**

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231, on October 24, 2000.

  
\_\_\_\_\_  
Gideon Gimlan, Reg. No. 31,955  
Signature Date: October 24, 2000 (Attorney Signature)

RESPONSE [A] TO OFFICE ACTION UNDER 37 C.F.R. § 1.111

Commissioner for Patents  
Washington, D.C. 20231

**RECEIVED**

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Sir:

TECHNOLOGY CENTER 2800

This RESPONSE [A] is in reply to the Office action mailed 07/05/00.

Amendments

Please amend the above-identified application as follows:

In the Specification,

Please amend the Specification as follows.

Page 1:

lines 15-16: Please delete "[Attorney Docket No. AMDI 8222]";

Page 2:

10/30/2000 CCHAU1 00000064 09235615  
02 FC:103 810.00 DP  
03 FC:102 240.00 DP

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